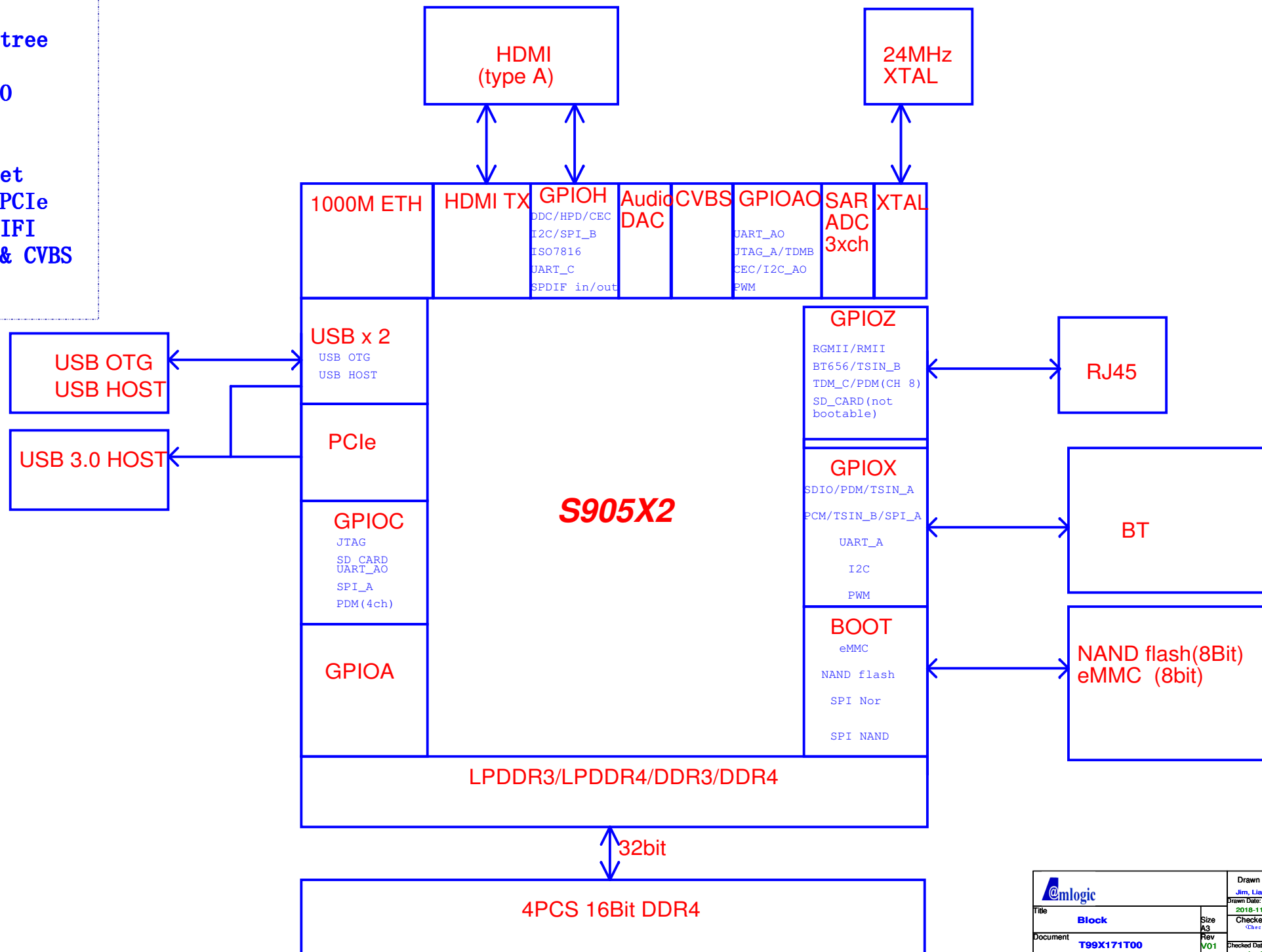
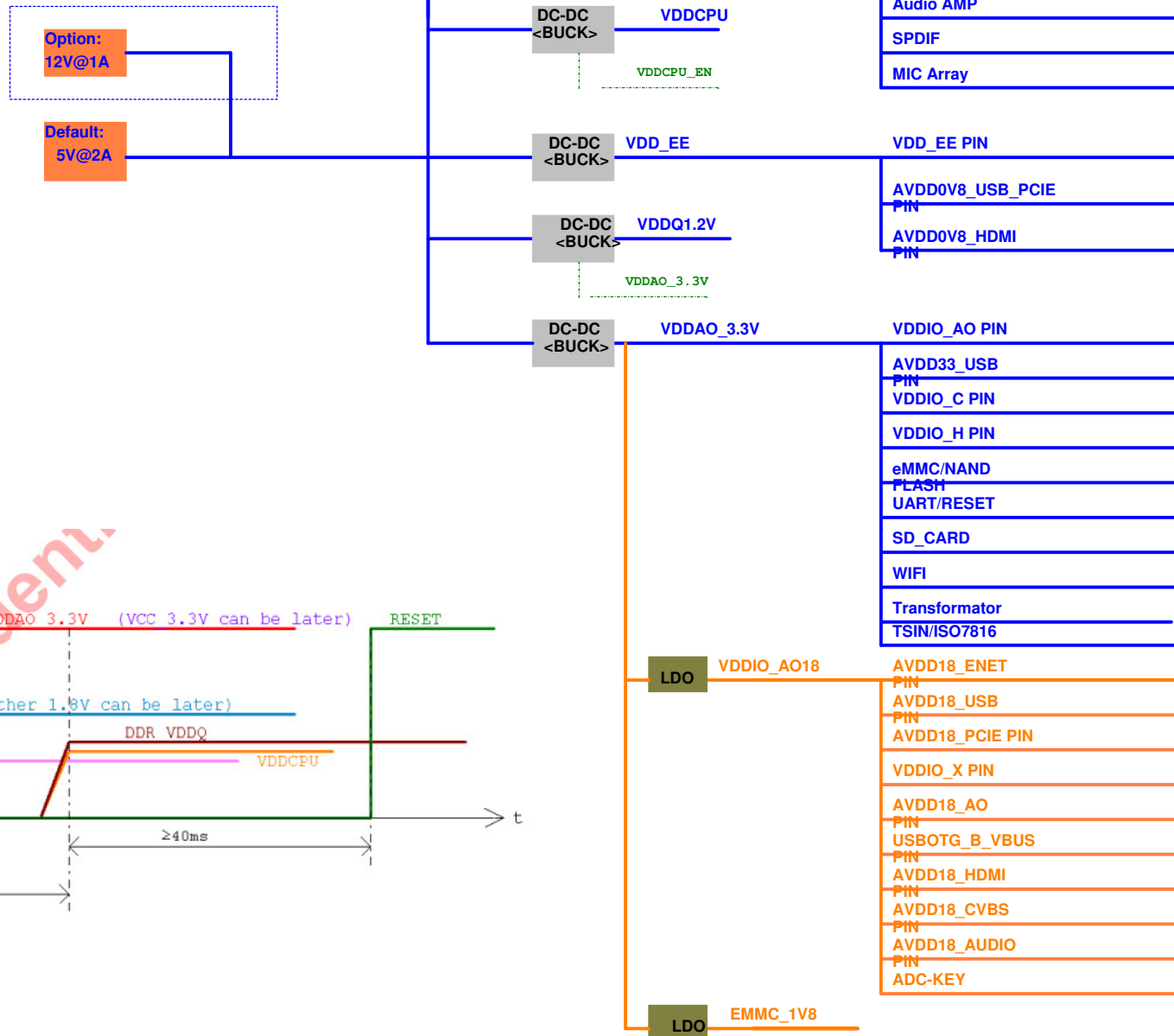


Page Index
 00- Block
 00- Power tree
 01- Power
 02- CPU I/O
 03- DDR4
 04- Flash
 05- Ethernet
 06- USB & PCIe
 07- SDIO WIFI
 08- Audio & CVBS
 09- HDMI

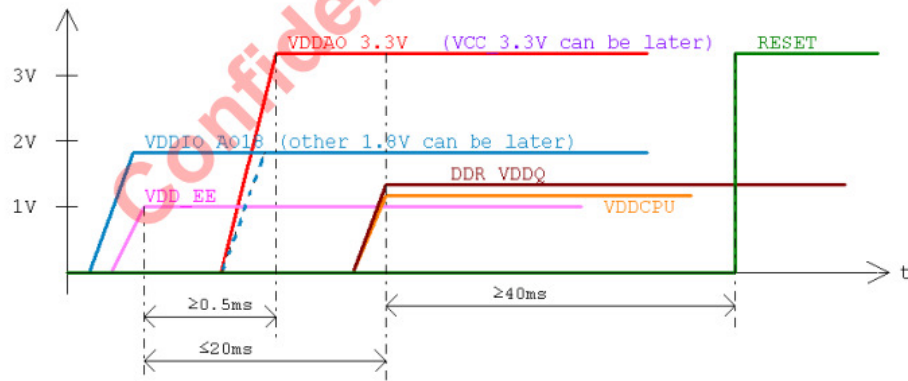
S905X2 REF BOARD DIAGRAM



Power Tree

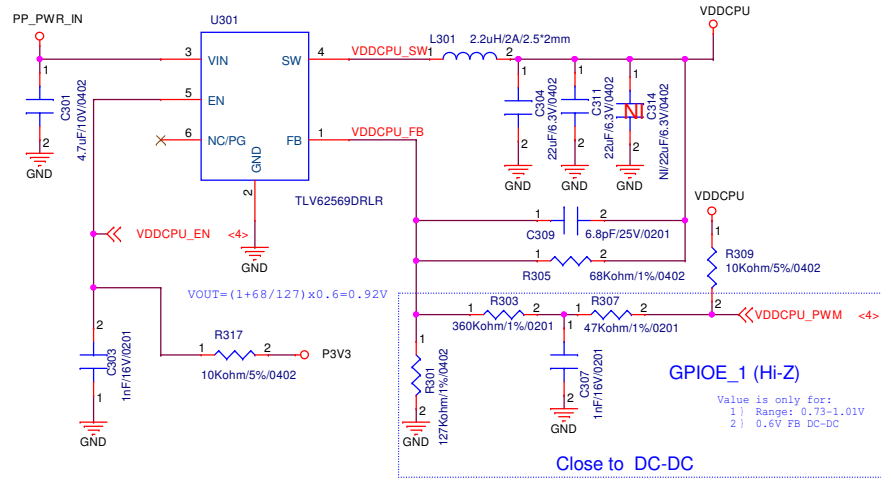


Example power on sequence:



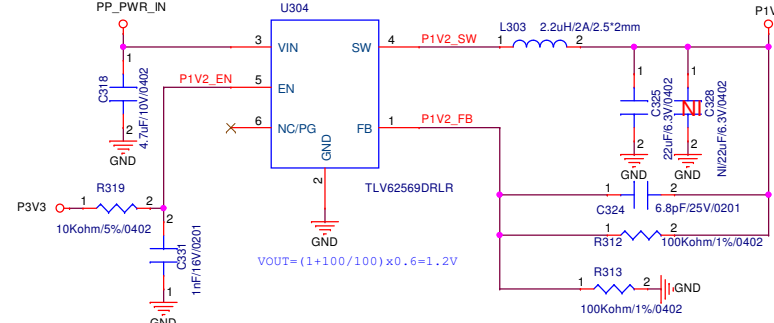
PP_PWR_IN to VDDCPU

Design Max: 2A



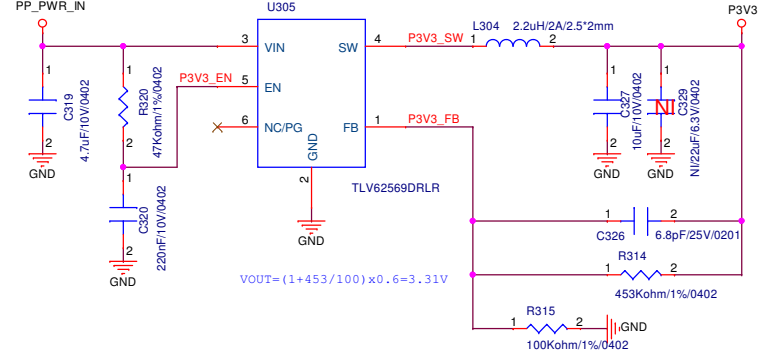
PP_PWR_IN to P1V2

Design Max: 2A



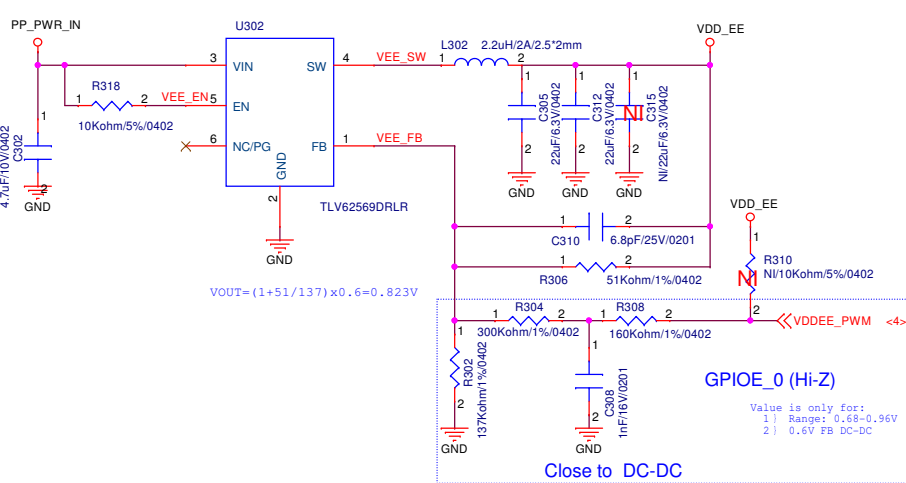
PP_PWR_IN to P3V3

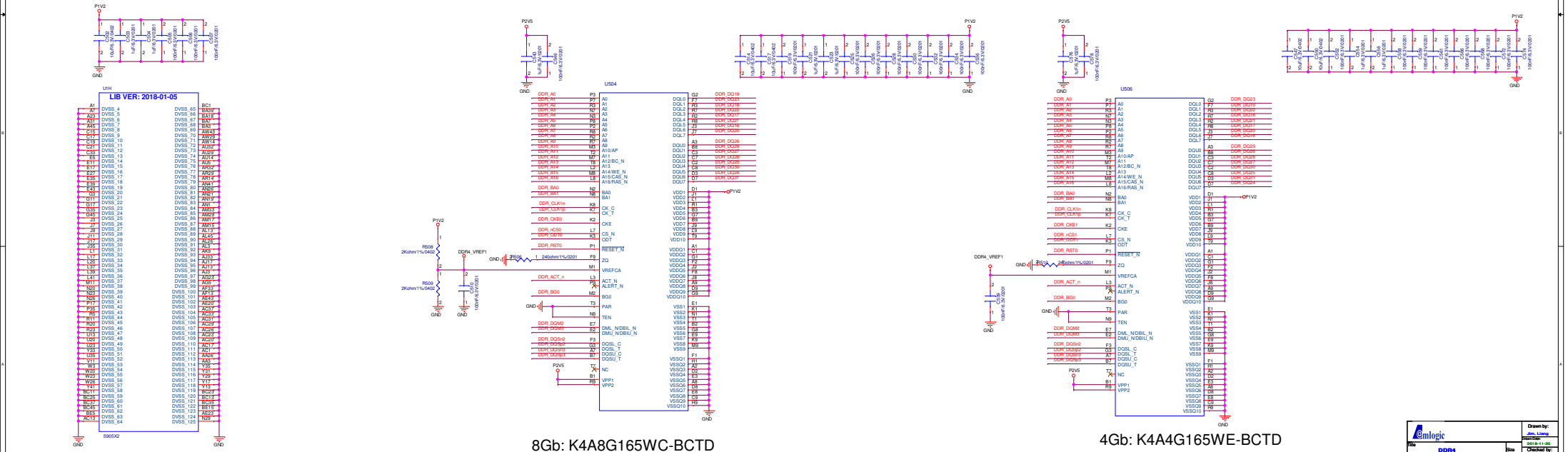
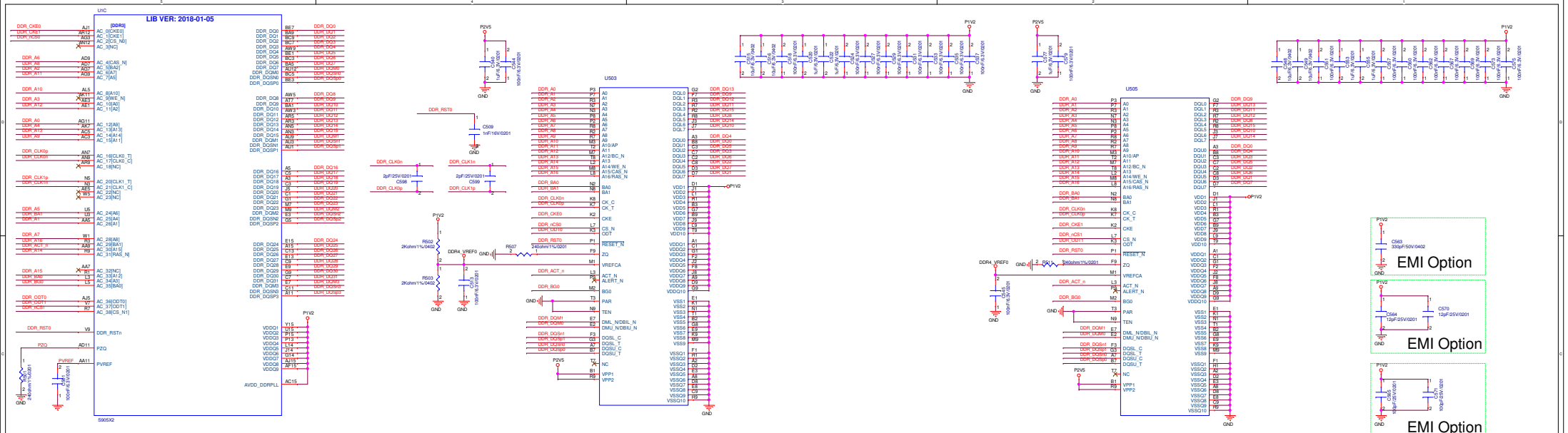
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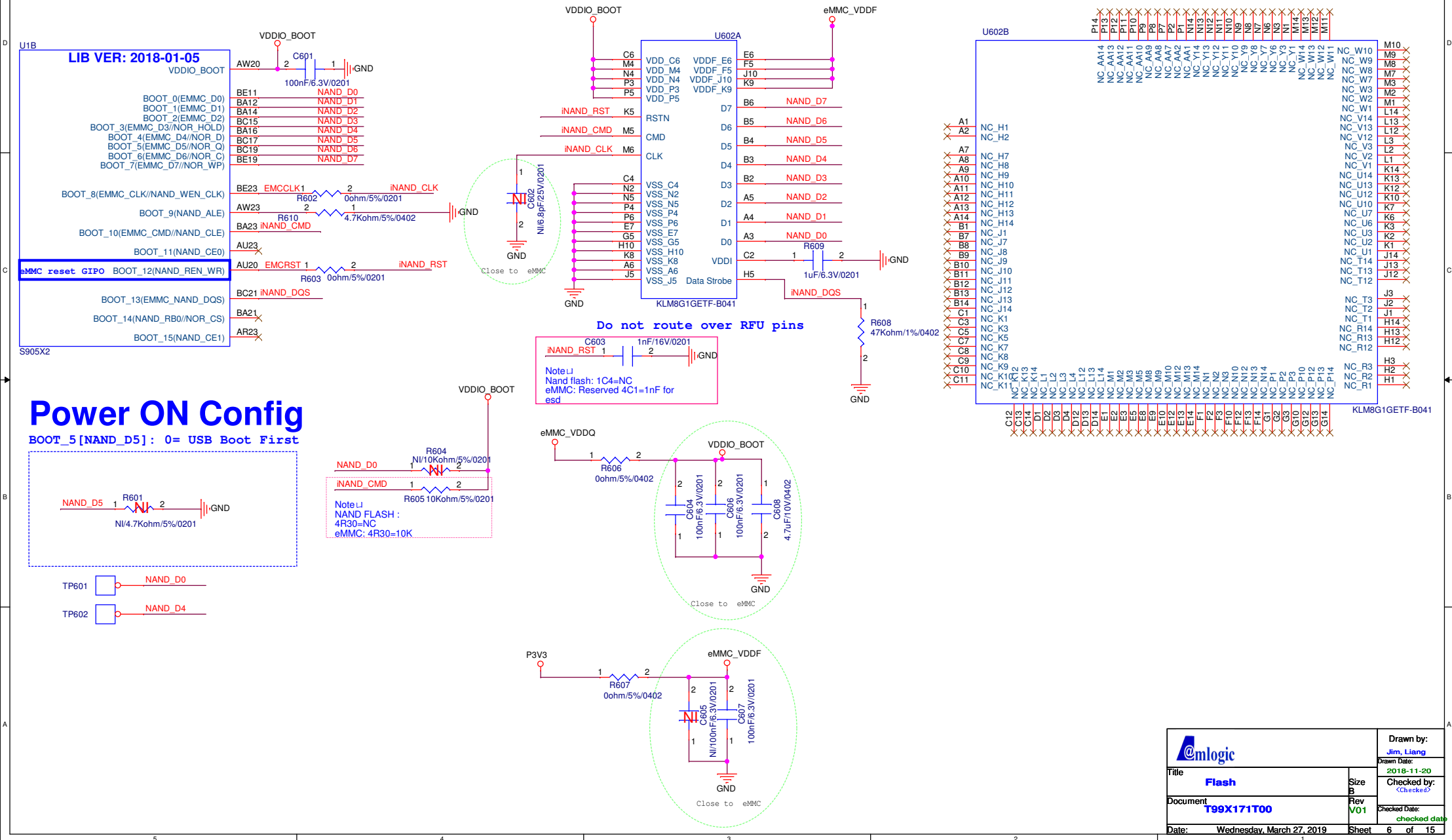
PP_PWR_IN to VDD_EE

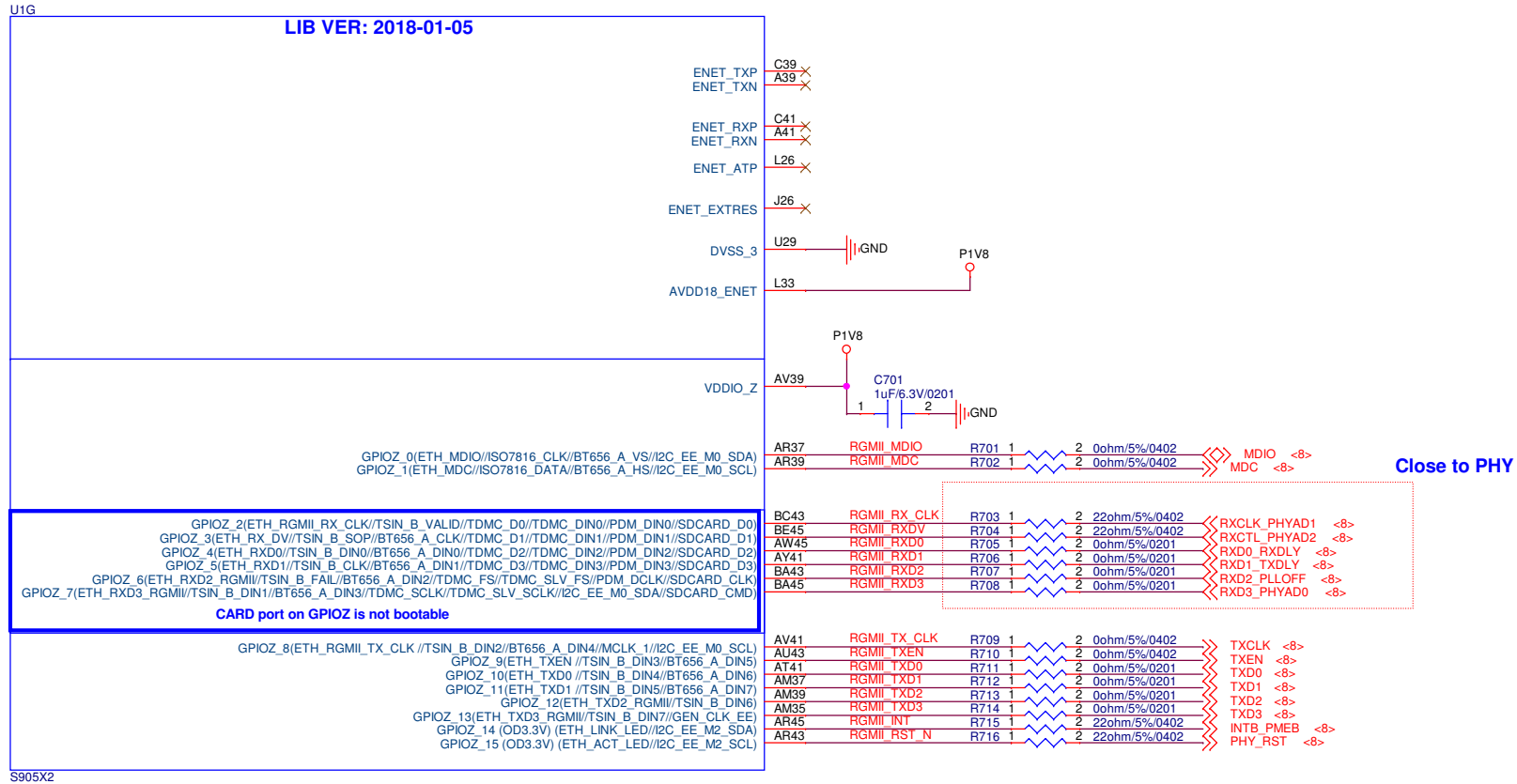
Design Max: 2A





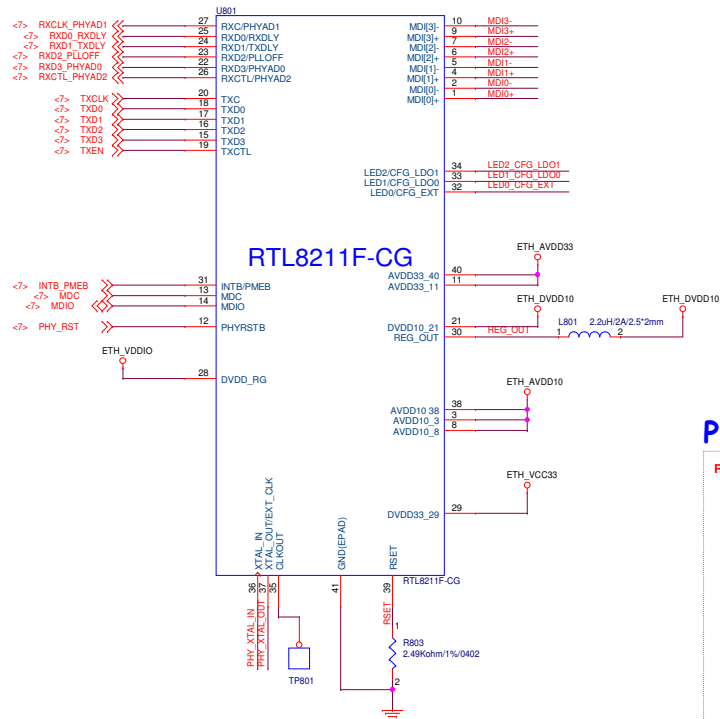
eMMC/iNAND



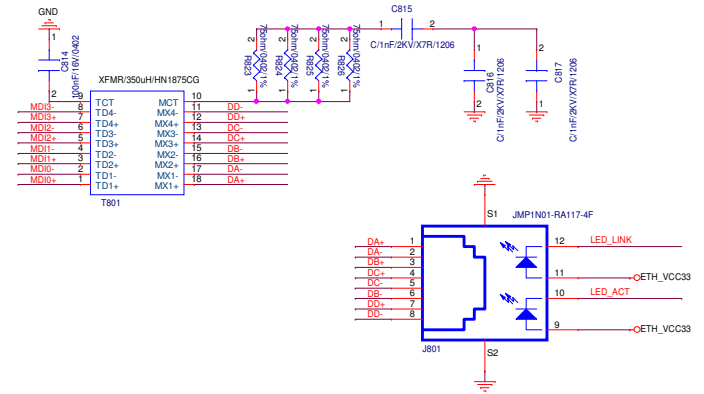
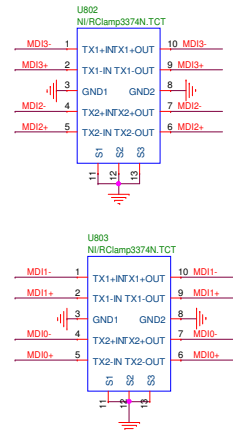


S905X2

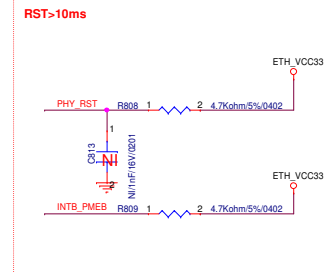
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Title Ethernet		Size B	Drawn Date: 2018-11-20
Document T99X171T00		Rev V01	Checked by: <Checked>
Date: Wednesday, March 27, 2019		Sheet 7	Checked Date: checked date
		of 15	



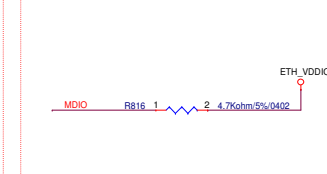
Transformer&RJ45 high-tension line



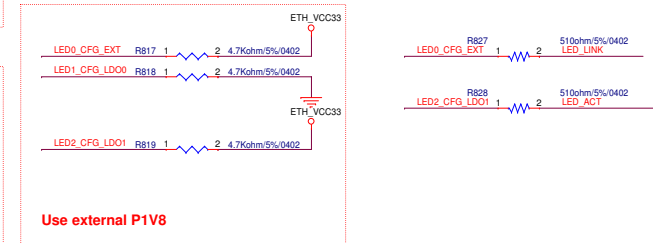
PHY_RST/INTB



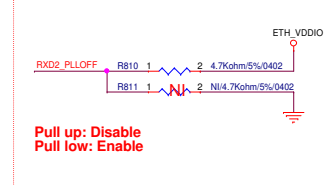
MDIO



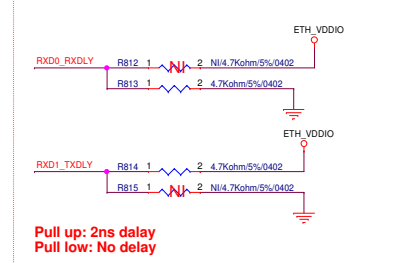
RGMII Voltage Config.



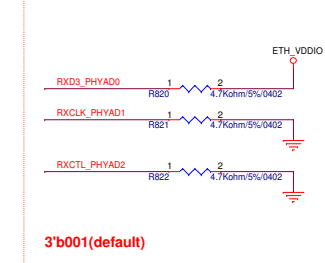
Disable/Enable PLL



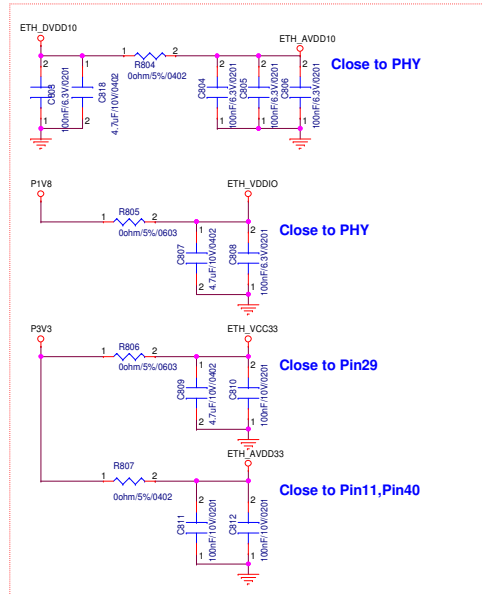
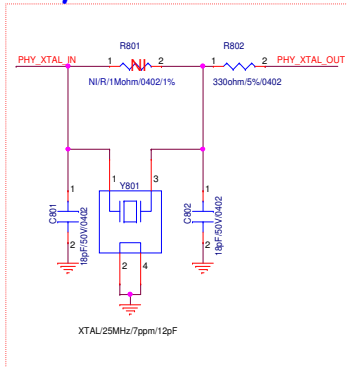
RGMII TXC/RXC Delay Config



PHY Address Config.



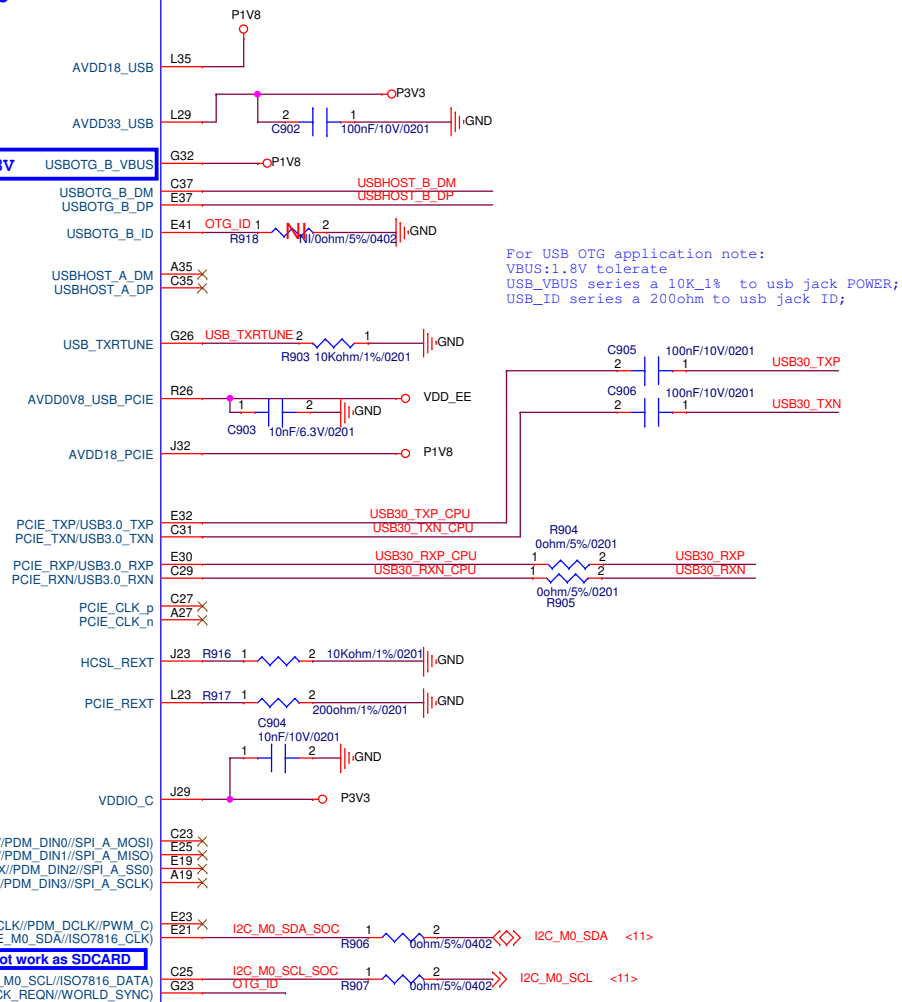
Crystal



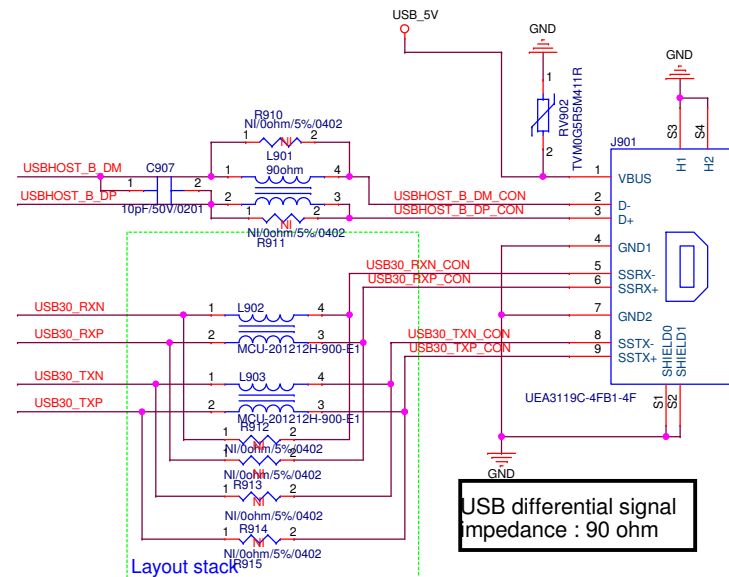
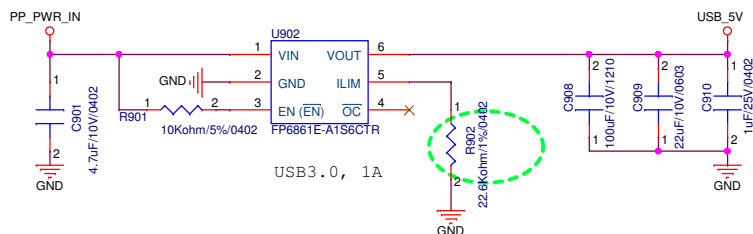
U1E

LIB VER: 2018-01-05

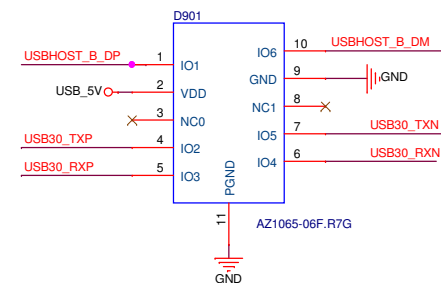
Tolerance 1.8V



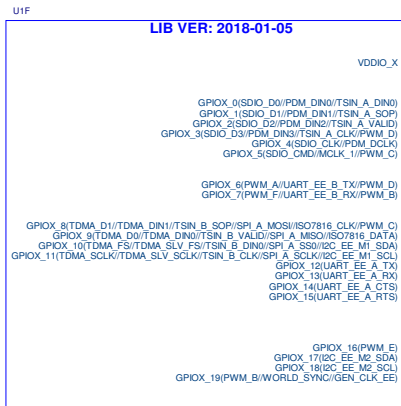
S905X2



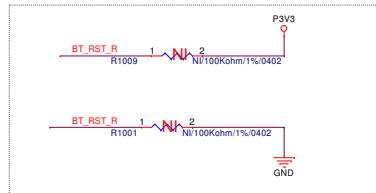
ESD



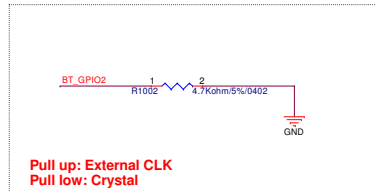
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		Drawn Date: 2018-11-20	
Title USB & PCIe		Checked by: Checked Date:	
Document T99X171T00		Size Custom	
Date: Wednesday, March 27, 2019		Rev V01	
		Sheet 9 of 15	



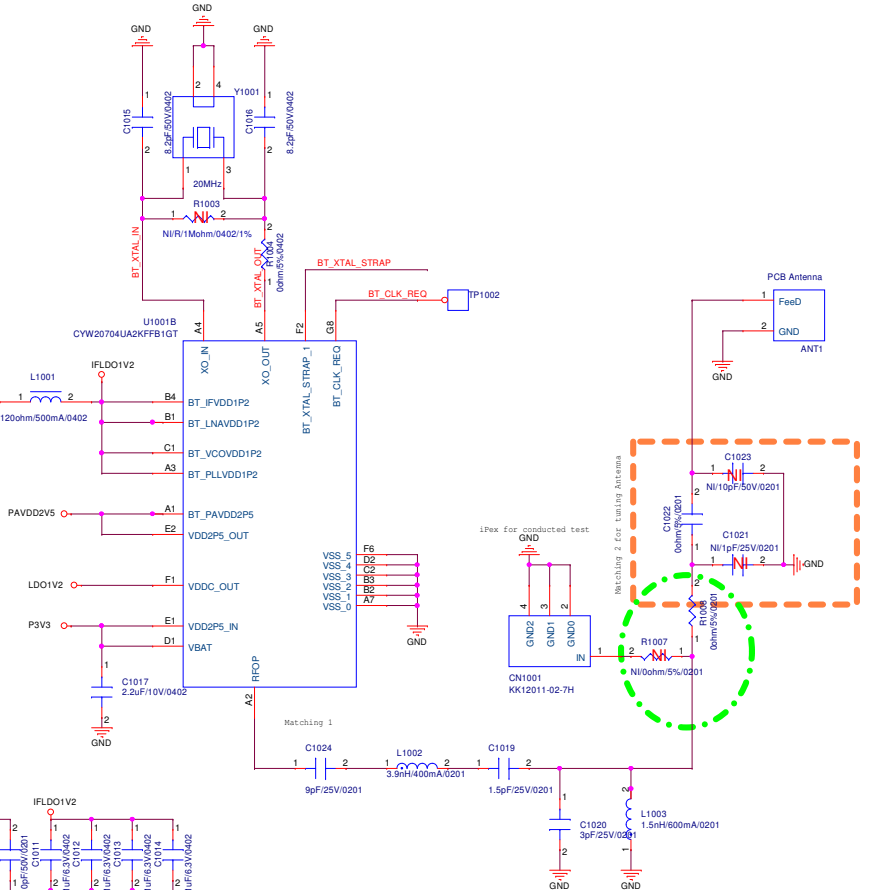
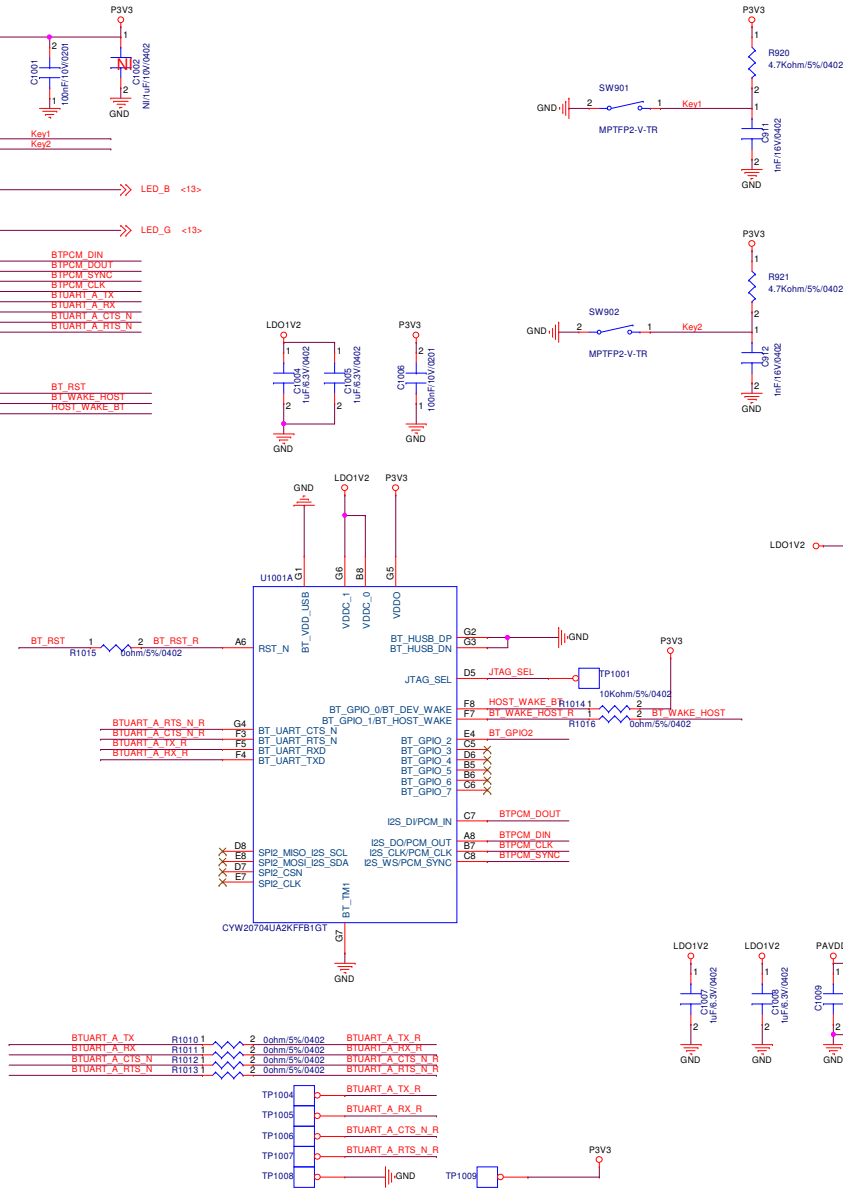
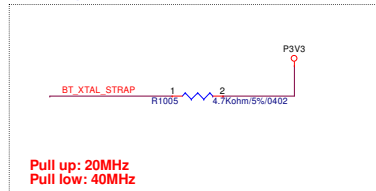
RST



CLK



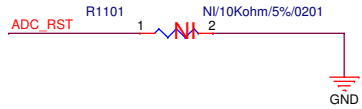
XTAL frequencies



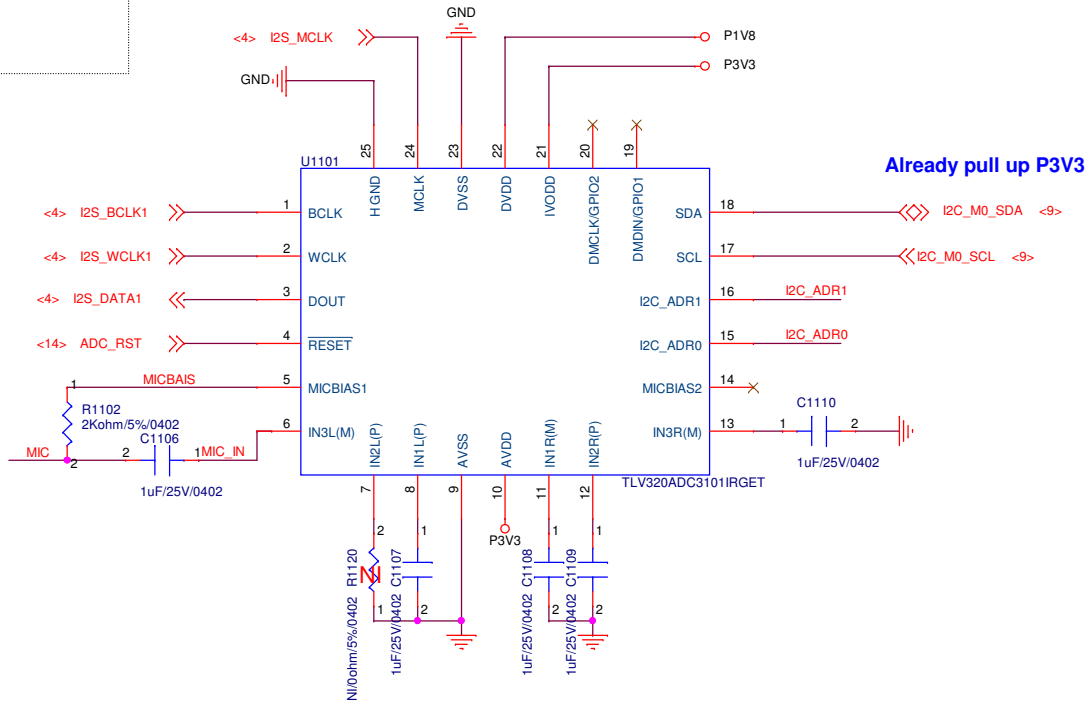
emlogic		Drawn by: Jem Liang
BT		Version: 2018-11-20
T99X171T00		Checked by: Jem Liang
Date: Wednesday, March 27, 2019		Sheet 10 of 15

ADC RESET

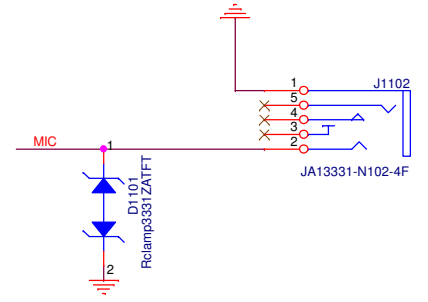
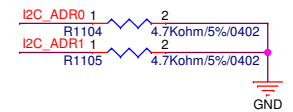
RST>10ns



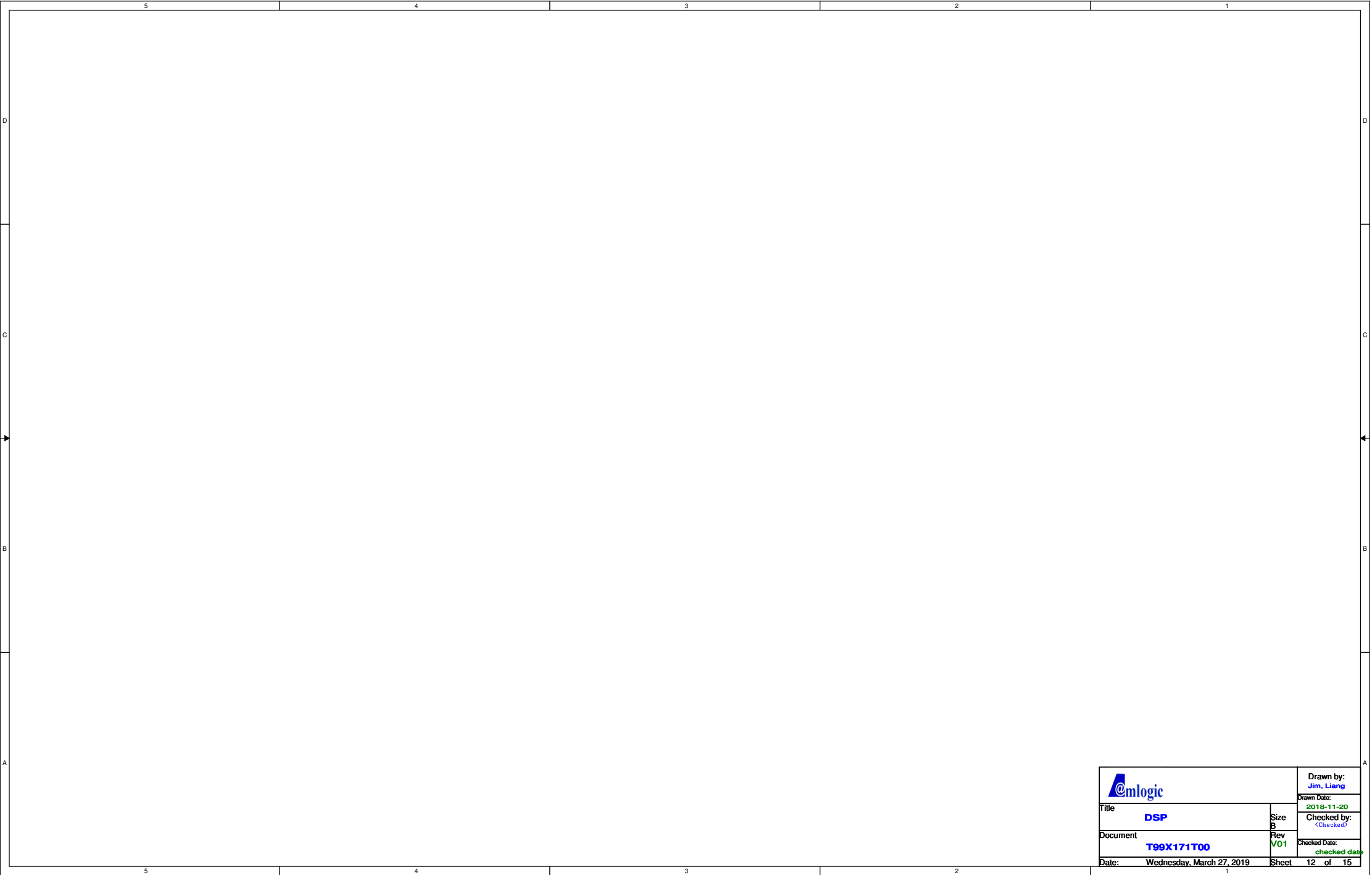
SLAVE



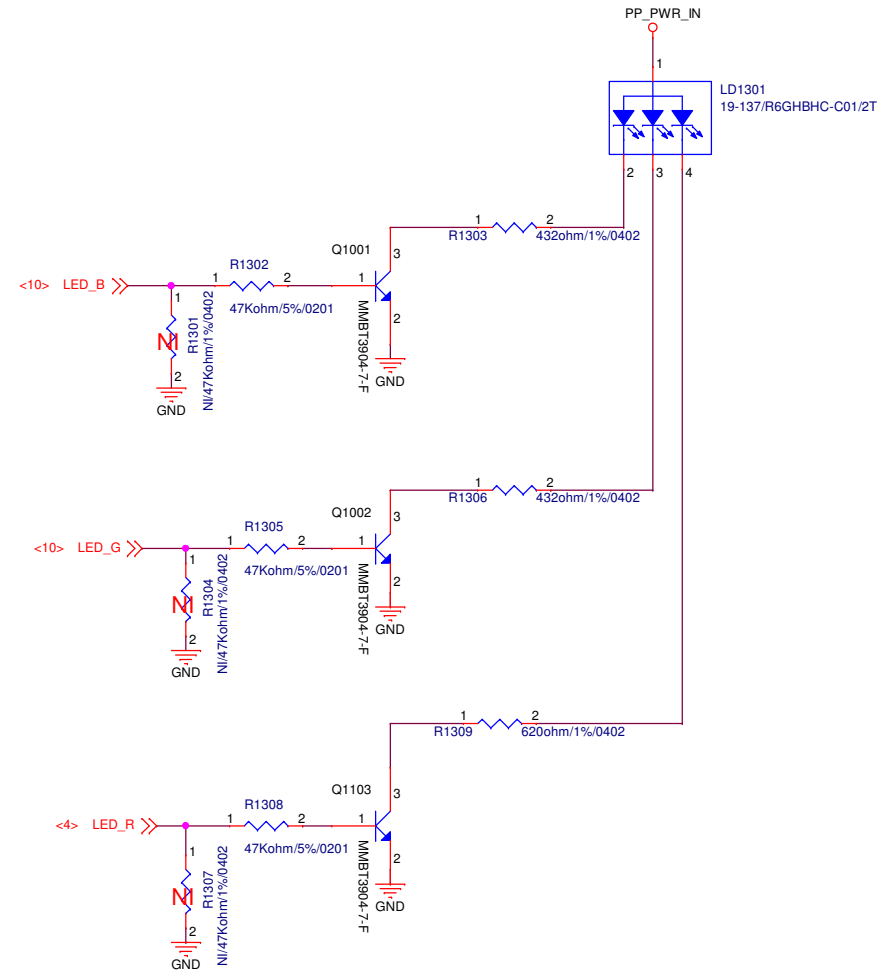
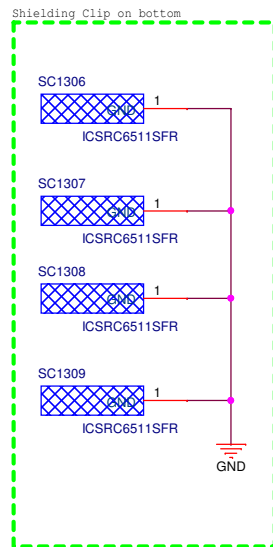
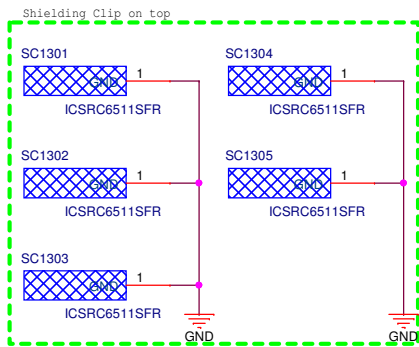
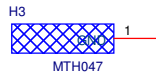
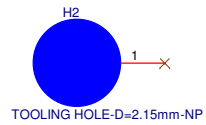
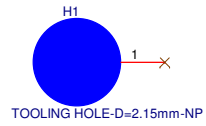
ADDRESS: 0x30



		Drawn by: Jlm, Liang	
Title ADC		Drawn Date: 2018-11-20	
Document T99X171T00		Checked by: <Checked>	
Date: Wednesday, March 27, 2019		Rev V01	
Sheet 11 of 15		Checked Date: checked date	



		Drawn by: Jim, Liang	
Title DSP		Size B	Drawn Date: 2018-11-20
Document T99X171T00		Rev V01	Checked by: <Checked>
Date: Wednesday, March 27, 2019		Sheet	12 of 15



		Drawn by: Jlm, Liang	
Title LED/CLIP		Size B	Drawn Date: 2018-11-20
Document T99X171T00		Rev V01	Checked by: <Checked>
Date: Monday, May 08, 2023		Sheet 13	Checked Date: checked date
		of	15

U1D

LIB VER: 2018-01-05

GPIOH_0 (OD5V) (HDMITX_SDA/I2C_EE_M3_SDA)
 GPIOH_1 (OD5V) (HDMITX_SCL/I2C_EE_M3_SCL)
 GPIOH_2 (OD5V) (HDMITX_HPD_IN/I2C_EE_M1_SDA)
 GPIOH_3 (OD5V) (I2C_EE_M1_SCL/AO_CEC_A/AO_CEC_B)

GPIOH_4 (SPDIF_OUT//UART_EE_C_RTS//SPI_B_MOSI)
 GPIOH_5 (SPDIF_IN//UART_EE_C_CTS//SPI_B_MISO//PWM_F//TDMB_D3//TDMB_DIN3)

GPIOH_6 (ISO7816_CLK//UART_EE_C_RX//SPI_B_SS0/I2C_EE_M1_SDA)
 GPIOH_7 (ISO7816_DATA//UART_EE_C_TX//SPI_B_SCLK/I2C_EE_M1_SCL)
 GPIOH_8 (OD5V)

VDDIO_H

GPIOH_4 (SPDIF_OUT//UART_EE_C_RTS//SPI_B_MOSI)
 GPIOH_5 (SPDIF_IN//UART_EE_C_CTS//SPI_B_MISO//PWM_F//TDMB_D3//TDMB_DIN3)

AVDD0V8_HDMI

AVDD18_HDMI

HDMI_CEXT

HDMI_REXT

DVSS_2

HDMITX_CK_P

HDMITX_CK_N

HDMITX_0P

HDMITX_0N

HDMITX_1P

HDMITX_1N

HDMITX_2P

HDMITX_2N

AVDD18_CVBS

CVBS_COMP

CVBS_VREF

CVBS_RSET

CVBS_IOUT

AVSS_CVBS

AVDD18_AUDIO

LOLP

LOLN

LORP

LORN

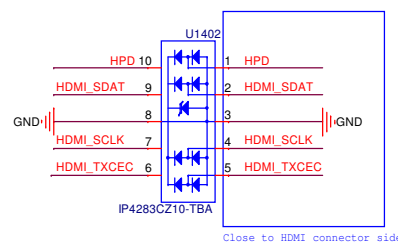
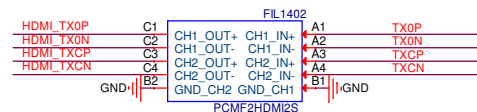
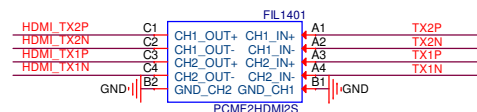
REFP

VMID

AVSS_AUDIO

S905X2

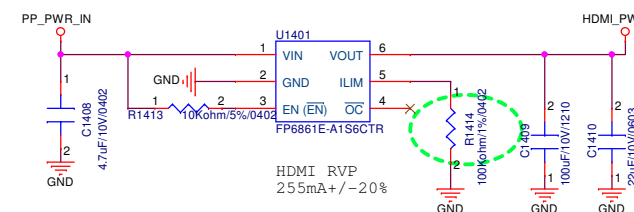
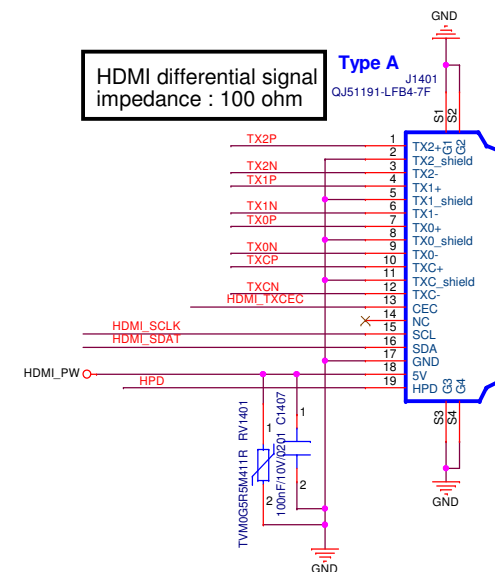
HDMI output



HDMI differential signal impedance : 100 ohm

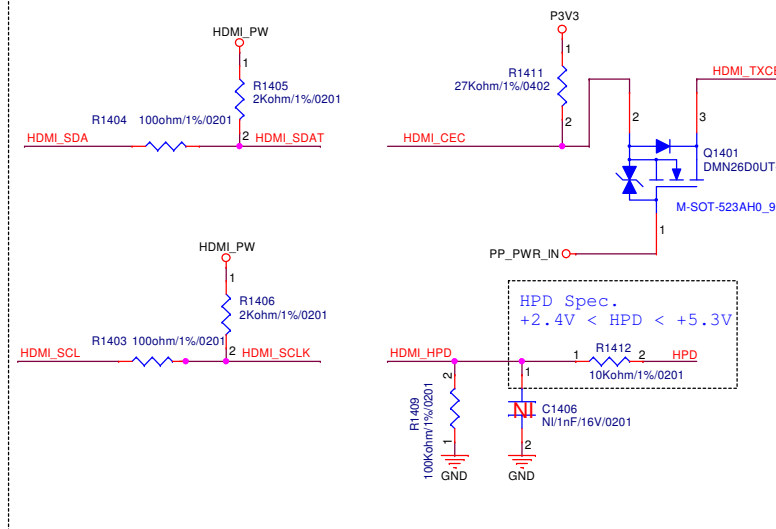
Type A

QJ51191-LFB4-7F



HDMI (power) Spec.
 $+4.8V < PVDD5 < +5.3V$

9Q2 防倒灌電路, 9R2/9R1 分壓電路不可刪除



		Drawn by: Jim, Liang	
Title HDMI		Drawn Date: 2018-11-20	
Document T99X171 T00		Checked by: (checked)	
Date: Wednesday, March 27, 2019		Rev V01	
Sheet 14 of 15		Checked Date: checked date	

Version	Change List	Date
001	First version of T99X171T00	2018/11/01

Version	Change List	Date
002	First version of T99X171T00	2019/03/15

- Page 3.
- 1. OVP and OCP: Change D301 and F301 to TPS25200 solution
 - 2. P1V8 LDO ripple: Change U303 and 306 from 027.01421.005 to JSTLV75518PDBV
 - 3. P2V5 LDO ripple: Change U303 and 306 from 027.01437.005 to JSTLV75525PDBV
- Page 4.
- 4. Slove I2S overshoot and undershoot:Change R412, R413, R414, R415 from 0ohm to 49.9ohm
 - 5. Support wake on BT: Change Net BT_WAKE_HOST fom GPIOX_18 to GPIOAO_2
- Page 7.
- 6. No use for reserve EMI: Delete C702 22p
- Page 8.
- 7. Xtal 25M: Change R802 from 0ohm to 330ohm
 - 8. For phy bringup: add C818 4.7u
 - 9. RGMII TXC/RXC Delay Config: Tx 2ns dealy, pop R814 and R815 nopop
Rx no dealy, pop R813 and R812 nopop
- Page 9.
- 10. USB OTG_ID control pin change to open drain pin: Change OUG_ID from GPIOC_1 to GPIOC_7
- Page 10.
- 11. Xtal 20M: Change C1015 and C1016 from 18p to 8.2p
 - 12. LED (B) change default pull up pin: change LED_B from GPIOAO_11 to GPIO_X5
 - 13. LED (G) change default pull up pin: change LED_G from GPIO_X6 to GPIO_X7
- Page 11.
- 14. ADC change AGND ro GND: Delete R1103, R1106, R1107, R1108, C1113
- Page 14.
- 15. Change HDMI I2C pull up from PP_PWR_IN to HDMI_PW